```
     FILE 'HCAPLUS' ENTERED AT 14:30:50 ON 27 APR 2004
L1          1251 S  (TWIN# OR TWINNED OR TWO OR PAIR#### OR DUAL?)(A)DAMASCENE#
L2           586 S  ANTIFUSE? OR ANTI(W)FUSE? OR FPIC OR FPGA
L3       1433460 S  VIA OR VIAS OR SPACE OR SPACES OR WINDOW# OR OPEN##### OR
                    INTERCONN?
L4        602528 S  PATTERN####
L5        591919 S  (ILD OR DIELECT##### OR INSULAT? OR NONCONDUCT? OR
                    NON(W)CONDUCT? OR DIELEC? OR INSULAT? OR OXIDE(W)(LAYER? OR
                    FILM##### OR COAT?))
L6             4 S  L1 AND L2 AND L3
L7          6661 S  L4(3A)L5
L8             1 S  L6 AND L7
L9             3 S  L6 NOT L8
```

Set	Items	Description
S1	755	(TWIN? ? OR TWINNED OR TWO OR PAIR???? OR DUAL?)(N)DAMASCENE? ?
S2	4989	ANTIFUSE? OR ANTI(W)FUSE? OR FPIC OR FPGA
S3	0	MC=(U11-C05G2A OR U11-D03B2? OR U12-C04 OR U14-D01A OR U14-A06B1)
S4	271	IC=(H01L-023/525)
S5	5161	S2:S4
S6	1130556	VIA OR VIAS OR SPACE OR SPACES OR WINDOW? ? OR OPEN????? OR INTERCONN?
S7	0	MC=(U11-C05D3 OR U11-C07D2 OR U11-C05G2 OR U11-D03B3 OR U11-D03C3 OR L04-C13B)
S8	998	IC=(H01L-021/88 OR H01L-023/535 OR H01L-023/538 OR H01L-021/88 OR H01L-021/90)
S9	1130828	S6:S8
S10	292074	PATTERN????
S11	**3**	**S1 AND S5 AND S9 AND S10(3N)(ILD OR DIELECT????? OR INSULAT? OR NONCONDUCT? OR NON(W)CONDUCT? OR DIELEC? OR INSULAT? OR OXIDE(W)(LAYER? OR FILM????? OR COAT?))**
S12	**4**	**S1 AND S5 AND S9 AND S10 NOT S11**

File 348:**EUROPEAN PATENTS** 1978-2004/Apr W02
(c) 2004 European Patent Office
File 349:**PCT FULLTEXT** 1979-2002/UB=20040415,UT=20040408
(c) 2004 WIPO/Univentio

File 350:**Derwent WPIX** 1963-2004/UD,UM &UP=200426
(c) 2004 Thomson Derwent

Set	Items	Description
S1	1179	(TWIN? ? OR TWINNED OR TWO OR PAIR???? OR DUAL?)(N)DAMASCENE? ?
S2	3916	ANTIFUSE? OR ANTI(W)FUSE? OR FPIC OR FPGA OR FIELD(3N)PROGRAM?????
S3	12218	MC=(U11-C05G2A OR U11-D03B2? OR U12-C04 OR U14-D01A OR U14-A06B1)
S4	332	IC=(H01L-023/525)
S5	15624	S2:S4
S6	2315721	VIA OR VIAS OR SPACE OR SPACES OR WINDOW? ? OR OPEN????? OR INTERCONN?
S7	31202	MC=(U11-C05D3 OR U11-C07D2 OR U11-C05G2 OR U11-D03B3 OR U11-D03C3 OR L04-C13B)
S8	12691	IC=(H01L-021/88 OR H01L-023/535 OR H01L-023/538 OR H01L-021/88 OR H01L-021/90)
S9	2342752	S6:S8
S10	361534	PATTERN????
S11	19	S1 AND S5 AND S9 AND S10(3N)(ILD OR DIELECT????? OR INSULAT? OR NONCONDUCT? OR NON(W)CONDUCT? OR DIELEC? OR INSULAT? OR OXIDE(W)(LAYER? OR FILM? OR COAT?))
S12	40	S1 AND S5 AND S9 AND S10
S13	3	S2 AND S12
S14	2	S13 NOT PN=US2001036750
S15	2	S14 NOT S11

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Set     Items   Description
S1       1539   (TWIN? ? OR TWINNED OR TWO OR PAIR???? OR DUAL?)(N)DAMASCENE? ?
S2      18011   ANTIFUSE? OR ANTI(W)FUSE? OR FPIC OR FPGA
S3    5739605   VIA OR VIAS OR SPACE OR SPACES OR WINDOW? ? OR OPEN????? OR
              INTERCONN?
S4       3513    PATTERN????(3N)(ILD OR DIELECT????? OR INSULAT? OR NONCONDUCT? OR
             NON(W)CONDUCT? OR DIELEC? OR INSULAT? OR OXIDE(W)(LAYER? OR FILM? OR
             COAT?))
S5          0   S1 AND S2 AND S3 AND S4
S6       1548   (TWIN? ? OR TWINNED OR TWO OR PAIR???? OR DUAL?)(2N)DAMASCENE? ?
S7      45711   ANTIFUSE? OR ANTI(W)FUSE? OR FPIC OR FPGA OR PROGRAM?(3N)FIELD
S8          0   S6 AND S7
File   2:INSPEC 1969-2004/Apr W3
         (c) 2004 Institution of Electrical Engineers
File   6:NTIS 1964-2004/Apr W4
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2004/Apr W2
         (c) 2004 Elsevier Eng.  Info. Inc.
File  25:Weldasearch 19662004/Nov
         (c) 2004 TWI Ltd
File  34:SciSearch(R) Cited Ref Sci 1990-2004/Apr W3
         (c) 2004 Inst for Sci Info
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  35:Dissertation Abs Online 1861-2004/Mar
         (c) 2004 ProQuest Info&Learning
File  65:Inside Conferences 1993-2004/Apr W4
         (c) 2004 BLDSC all rts. reserv.
File  94:JICST-EPlus 1985-2004/Apr W2
         (c)2004 Japan Science and Tech Corp(JST)
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Mar
         (c) 2004 The HW Wilson Co.
File 103:Energy SciTec 1974-2004/Apr B1
         (c) 2004 Contains copyrighted material
File 144:Pascal 1973-2004/Apr W3
         (c) 2004 INIST/CNRS
File 239:Mathsci 1940-2004/Jun
         (c) 2004 American Mathematical Society
File 241:Elec. Power DB 1972-1999Jan
         (c) 1999 Electric Power Research Inst.Inc
File 305:Analytical Abstracts 1980-2004/Apr W2
         (c) 2004 Royal Soc Chemistry
File 315:ChemEng & Biotec Abs 1970-2004/Mar
         (c) 2004 DECHEMA
File 354:Ei EnCompassLit(TM) 1965-2004/Apr W2
         (c) 2004 Elsevier Eng. Info. Inc.
File 987:TULSA (Petroleum Abs) 1965-2004/Apr W4
         (c)2004 The University of Tulsa
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15/9/1

DIALOG(R)File 350:**Derwent WPIX**

013465697 WPI Acc No: 2000-637640/200061

Fabrication of **anti-fuse** module and **dual damascene interconnect** structure involves forming metal line, depositing and **patterning** silicon nitride and fusing element layers, and forming **anti-fuse** metal line and **interconnect**

Patent Assignee: CHARTERED SEMICONDUCTOR MFG LTD PTE (CHAR-N)

Inventor: CHU S S; LEE C; SHAO K; XU Y

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6124194	**A**	**20000926**	**US 99439365**	**A**	**19991115**	**200061**	**B**

Abstract (Basic): US 6124194 A

NOVELTY - An **anti-fuse** module and **dual damascene interconnect** structure is fabricated by forming a first metal line, depositing and **patterning** silicon nitride layer, depositing and **patterning** a fusing element layer, and simultaneously forming an **anti-fuse** line and a **dual damascene interconnect** on and contacting with a second metal line.

DETAILED DESCRIPTION - An **anti-fuse** module and **dual damascene interconnect** structure is fabricated by forming a first metal **via** within a first dielectric layer (20) within an **anti-fuse** area (16) and contacting a first metal line (12); depositing a silicon nitride (SiN) layer on the dielectric layer and metal **via** (26); **patterning** the SiN layer (28) to form at least two **openings**; depositing and **patterning** a fusing element layer on the **patterned** SiN layered structure to form a fusing element on the metal **via**; and simultaneously forming an **anti-fuse** metal line (56) on the fusing element (44) to form an **anti-fuse** module within the **anti-fuse** area, and a **dual damascene interconnect** (58) and contacting with a second metal line and within the **interconnect** area (18). A first **opening** exposes the first metal **via** and a second **opening** exposes a portion of the first dielectric layer above the second metal line (14).

USE - For fabricating an **anti-fuse** module and **dual damascene interconnect** structure.

ADVANTAGE - The invention can be used with a **dual damascene** process without damaging the **via** portion of the **dual damascene interconnect** structure. The module is on a smaller design rule because a **dual damascene** process provides a very advanced design for local **interconnections.**

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional representation of the invention.

First metal line (12)
Second metal line (14)
Anti-fuse area (16)
Interconnect area (18)
First dielectric layer (20)
Metal **via** (26)
SiN layer (28)
Tantalum nitride (36)
Amorphous silicon (38)
Fusing element (44)
Anti-fuse metal line (56)

Dual damascene interconnect (58)
Technology Focus:
TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Material: The first metal **via** comprises metal from tungsten, aluminum, or copper. The fusing element layer and fusing element comprise a lower layer of tantalum nitride (36), a middle layer of amorphous silicon (38), and an upper layer of tantalum nitride. The first dielectric material comprises a low dielectric constant material. The **anti-fuse** metal line and **dual damascene interconnect** is formed from copper.
Title Terms: FABRICATE; ANTI; FUSE; MODULE; DUAL; **INTERCONNECT**; STRUCTURE; FORMING; METAL; LINE; DEPOSIT; **PATTERN**; SILICON; NITRIDE ; FUSE; ELEMENT; LAYER; FORMING; ANTI; FUSE; METAL; LINE; **INTERCONNECT**
Derwent Class: L03; U11
International Patent Class (Main): H01L-029/00
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C10A; **L04-C13B**
Manual Codes (EPI/S-X): **U11-C05D3; U11-C05G2A**; U11-C05G2C; **U11-D03B2A**

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15/9/2
DIALOG(R)File 350:**Derwent WPIX**

011153888 WPI Acc No: 1997-131812/199712 Related WPI Acc No: 1998-086264
Dual damascene anti-fuse structure mfr. with reduced cost - including deposition of process control layer over **anti-fuse** structure and etching of **opening** in process control layer, etc.
Patent Assignee: CHARTERED SEMICONDUCTOR MFG LTD PTE (CHAR-N); CHARTERED SEMICONDUCTOR MFG PTE LTD (CHAR-N)
Inventor: CHAN L; ZHENG J Z; ZHENG J

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5602053	**A**	**19970211**	**US 96628068**	**A**	**19960408**	**199712**	**B**
SG 52951	A1	19980928	SG 971108	A	19970408	199904	

Abstract (Basic): US 5602053 A
Mfr. of an **antifuse** structure comprises: (a) providing a 1st conductive layer; (b) depositing a 1st insulating layer on the 1st conductive layer; (c) **patterning** and etching the 1st insulating layer to form a trench; (d) **patterning** and etching the 1st insulating layer, including the trench to form a cavity extending from inside the trench down to the level of the 1st conductive layer; (e) depositing a barrier layer on the 1st insulating layer and on all walls of the trench and the cavity; (f) depositing a 2nd conductive layer so as to more than fill the cavity and the trench; (g) removing the 2nd conductive layer and the barrier layer as far as the level of the 1st insulating layer to form a 1st **dual damascene** connector (DDC) having an upper surface; (h) depositing a 1st layer of Si nitride on the **antifuse** structure; (i) depositing a 1st layer of amorphous Si on the nitride layer; (j) depositing a 2nd layer of Si nitride on the 1st layer of amorphous Si; (k) depositing a 2nd layer of amorphous Si on the 2nd layer of nitride; (l) **patterning** and then etching the 1st and 2nd layers of Si nitride and amorphous Si to form a pedestal that overlaps the 1st DDC; (m) depositing a 2nd insulating layer on the 1st insulating layer and on the 2nd layer of amorphous Si; and (n) forming a 2nd DDC that extends through the 2nd insulating layer

See HCAPLUS HIT L9 #3

down to and making electrical contact with the 2nd layer of amorphous Si.

Also claimed is a process as above further comprising between steps (g) and (h), the deposition of a process control layer over the **antifuse** structure and the etching of an **opening** in the process control layer to fully expose the upper surface of the DDC.

USE - **Antifuse** structure for programmable logic and memory devices.

ADVANTAGE - Fewer mfg. steps, reduced costs and improved reliability i.e. all electrically active surfaces of the **antifuse** structure are planar.

Dwg.5/6

Title Terms: DUAL; ANTI; FUSE; STRUCTURE; MANUFACTURE; REDUCE; COST; DEPOSIT; PROCESS; CONTROL; LAYER; ANTI; FUSE; STRUCTURE; ETCH; **OPEN** ; PROCESS; CONTROL; LAYER

Index Terms/Additional Words: PROGRAMMABLE; MEMORY; LOGIC; DEVICE

Derwent Class: L03; U11

International Patent Class (Main): H01L-021/70

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L03-G04A; L04-C14

Manual Codes (EPI/S-X): **U11-C05G2A; U11-D03B2A**

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11/3,k/2 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00895724 **Image available**
HIGH-DENSITY METAL CAPACITOR USING **DUAL-DAMASCENE** COPPER **INTERCONNECT**

Patent Applicant/Assignee:
BROADCOM CORPORATION, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US
Patent Applicant/Inventor:
TSAU Liming, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US
Patent and Priority Information (Country, Number, Date):
Patent: **WO 200229892** A2-A3 20020411 (WO 0229892)
Application: WO 2001US31140 20011003 (PCT/WO US0131140)
Priority Application: **US 2000237916** 20001003

English Abstract
An electronic structure having a first conductive layer provided by a **dual damascene** fabrication process; an etch-stop layer provided by the fabrication process, and electrically coupled with the first conductive layer, the etch-stop layer having a...
...geometry; and a second conductive layer, electrically coupled with the etch-stop layer. The structure can be, for example, a metal-insulator-metal capacitor, an **antifuse**, and the like.

Detailed Description
I HIGH-DENSITY METAL CAPACITOR USING
DUAL-DAMASCENE COPPER **INTERCONNECT**
BACKGROUND OF THE MENTION
1 Field of the Invention
The invention herein relates to the formation of an integrated circuit including a capacitor.

.10 2 Description of the Related Art

Single damascene is an **interconnection** fabrication process in which grooves are formed in an insulating layer and filled with metal, for example, copper, to form the conductive lines. **Dual damascene** is a multi-level **interconnection** process in which conductive **via openings** are formed in addition to forming the grooves of single **damascene**. **Dual damascene** is an improvement over single damascene because it permits the filling of both the conductive grooves and **vias** with metal at the same tipe, thereby eliminating process steps. Because a **dual damascene** structure satisfies the requirement of low resistance and high electromigration, it has been widely used in deep sub-micron VLSI fabrication processes for obtaining an efficient and reliable **interconnections**. hi fabricating very and ultra large scale integration (VLSI and ULS1) circuits with the copper **dual damascene** process, insulating or **dielectric** materials are **patterned** with several thousand **openings** for the conductive lines and **vias**, which are filled at the same time with metal, and serve to **interconnect** the active and/or passive elements of the integrated circuit.

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11/3,k/3 (Item 2 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00807604 **Image available**
IMPROVED FLOURINE DOPED SIO2 FILM
Patent Applicant/Assignee:
INTEL CORPORATION, 2200 Mission College Boulevard, Santa Clara, CA 95052,
Patent Applicant/Inventor:
CHOI Chi-hing, 5581 NW O'Day Place, Portland, OR 97229, US, US
BUMGARNER John, 3302 NE Olympic Street, Hillsboro, OR 97124, US, US
WILKE Todd, 250 SW 90th Avenue, Portland, OR 97225, US, US (Residence),
BOST Melton, 555 N.E. Joyce Court, Hillsboro, OR 97124-2133, US, US
Patent and Priority Information (Country, Number, Date):
Patent: **WO 200141203** A1 20010607 (WO 0141203)
Application: WO 2000US28164 20001011 (PCT/WO US0028164)
Priority Application: **US 99451464 19991130**

Detailed Description
... Flourine doped silicon dioxide (SiO2) has been proposed as an intermetal dielectric because of its low dielectric constant and its ease of intregration into current **interconnection** processing.
A current method of forming a flourine doped S'02 layer in order to meet gap fill requirements for sub n-dcron processes is...

...the present invention over the substrate of Figure 1.

Figure 4 is an illustration of a cross-sectional view showing the planarization and formation of **via openings** in the substrate of Figure 3.

Figure 5 is an illustration of a cross-sectional view showing the filling of the **via openings** in the substrate of Figure 4 with a conductive material.

Figure 6 is an illustration of a cross-sectional view showing the formation of a...

...incorporated into the film.

Additionally, since the film can be formed by a high density plasma process it can fill high aspects ratio gaps or **openings**.

The flourine doped nitrogen containing silicon dioxide film of the present invention is ideally suited for use as an intermetal dielectric in the fabrication of...

...device.

The present invention is described with respect to the formation of an intermetal dielectric onto the substrate 100 in order to isolate the metal **interconnect** lines 116 of the first level of metalization (e.g. metal 1) from a ...semiconductor substrates such as those used in the fabrication of memory devices such as DRAMs and EEPROMs or other types of logic devices such as **FPGA**'s and ASCIC's and can be used on other types of substrates such as those used for flat panel displays. In short the process...

Although one technique for forming **via** as **interconnects** in an
on ILD 120
has been described, other well known techniques such as damascene and
dual damascene can be used if desired. The above described
flourine doped nitrogen containing silicon oxide film formation process
and **via/ interconnect** formation process can be continued to
provide additional levels of metalization. and isolation as desired.

A method for forming a low dielectric constant silicon dioxide...
...lines 116) and between levels of metalization (e.g., metal 1 and metal
2). The dielectric film 120 can be deposited into high aspect ratio
opening (aspect ratios as high as 3.5:1).

Additionally, because the film includes a small amount of nitrogen, the
film
exhibits excellent moisture resistance and...

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12/3,k/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01640730
Memory structures
PATENT ASSIGNEE:
Hewlett-Packard Company, (206037), 3000 Hanover Street, Palo Alto, CA
INVENTOR:
Fricke, Peter, 7101 Rhoda Way, Crovallis, OR 97330, (US)
Koll, Andrew, 937 5th Avenue SW, Albany, OR 97321, (US)
Lazaroff, Dennis M., 2296 NW Nightingale Place, Corvallis, OR 97330, (US)
Van Brocklin, Andrew L., 6050 NW Happy Valley Drive, Corvallis, OR 97330,
PATENT (CC, No, Kind, Date): **EP 1351253** A1 031008 (Basic)
APPLICATION (CC, No, Date): EP 2003252043 030331;
PRIORITY (CC, No, Date): **US 115750 020402**

...SPECIFICATION a lesser amount of energy to the memory cell and sensing
whether current flows through the cell.
The memory storage element 23 can be an **antifuse** device, such as
a programmable tunnel junction device. The **antifuse** device can be
either a dielectric rupture type device or a tunnel junction device. The
tunnel junction can be formed from oxidized metal, thermally grown...
...and 6 schematically depict an embodiment of a memory structure that
includes memory cells each including a memory storage element 23 disposed
between a conductive **via** or pillar 233 and an edge of a horizontal
conductive plate 239a. A non-horizontal conductive panel 239b is
connected to and laterally adjacent the...

...an elongated conductive wall 635 that has a vertical extent and is
laterally and laminarly adjacent the non-horizontal conductive panel
639b. A vertical conductive **via** or pillar 641 is disposed in the
conductive tub 633 and contacts the tub at an **opening** in the base
of the conductive tub, for example. The conductive pillar 641 and the
conductive tub 633 form a conductive structure having a vertical...The
disclosed memory structures can be implemented using semiconductor
equipment. For example, the conductors can be formed by deposition of a
metal layer followed by **patterning** by photolithographic masking and

etching. Dielectric regions can be formed by deposition of dielectric material, while oxide layers can be formed by deposition of an...
...or oxidation of a metal feature. Chemical mechanical polishing (CMP) can be employed to planarize and/or expose desired regions. Also, damascene processes such as **dual damascene** can be employed. In **dual damascene** processes, ILD is etched, metal is deposited on the etched ILD, and CMP is performed.

Referring now to FIG. 19, the disclosed structures can generally be made as follows. At 101 a first electrode is created for example by depositing and **patterning** a metal layer. At 103 a control element is formed on the first electrode, for example by oxidizing the electrode or forming an unpatterned oxide layer as described above. At 105 a second electrode having an edge is created, for example by depositing and **patterning** a metal layer. At 107 a memory storage element is formed on the edge of the second electrode, for example by oxidizing the electrode or...

...CLAIMS memory structure of claim 1, 2, 3, 4, 5, 6 or 7 wherein said memory storage element is selected from the group consisting of an **antifuse**, a fuse, a charge storage device, a resistive material, a trap-induced hysteresis material, a ferroelectric capacitor material, a Hall effect material, and a tunneling...

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11/3,AB,DE/1
DIALOG(R)File 350:**Derwent WPIX**

015459456
WPI Acc No: 2003-521598/200349
Related WPI Acc No: 2003-438949
Copper damascene structure formation method, for semiconductor device, involves forming tungsten nitride layer in contact with **opening** formed by directly **patterning** low-**dielectric** constant layer
Patent Assignee: AHN K Y (AHNK-I); FORBES L (FORB-I)
Inventor: AHN K Y; FORBES L

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030020180	**A1**	**20030130**	**US 2001910914**	**A**	**20010724**	**200349**	**B**

Abstract (Basic):

NOVELTY - A low-dielectric constant layer (55) is directly patterned to form an **opening** in which a copper layer is provided. A tungsten nitride layer is formed in contact with the **opening** by atomic layer deposition using sequential surface reactions.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(1) the **dual damascene** structure; and

(2) processor-based system comprising a processor coupled to an integrated circuit, at least one of which contains the damascene structure.

USE - Formation of copper damascene structure in semiconductor devices.

ADVANTAGE - Suppresses diffusion of copper atoms into underlying damascene layers. Sequential photo resist/mask/etch steps and etch-stop layers are eliminated, production costs are reduced and productivity is increased.

DESCRIPTION OF DRAWING(S) - The figure shows a cross sectional view of a semiconductor device.

Copper layer (52)
Dielectric layer (55)
Diffusion barrier layer (72)
pp; 16 DwgNo 17/18

Title Terms: COPPER; STRUCTURE; FORMATION; METHOD; SEMICONDUCTOR; DEVICE; FORMING; TUNGSTEN; NITRIDE; LAYER; CONTACT; **OPEN**; FORMING; PATTERN; LOW; DIELECTRIC; CONSTANT; LAYER

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11/3,AB,DE/2
DIALOG(R)File 350:**Derwent WPIX**

014918916
WPI Acc No: 2002-739623/200280
Electrical metal fuse production comprises forming first **patterned dielectric** layer on substrate, first planarized structure, second **patterned dielectric** layer, and second planarized structure
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: YU T

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6444503	**B1**	**20020903**	**US 200268922**	**A**	**20020207**	**200280**	**B**

Abstract (Basic):

NOVELTY - An electrical metal fuse is formed by forming a first **patterned dielectric** layer on a substrate having first **opening**(s), forming a first planarized structure in the first **opening**, forming a second **patterned dielectric** layer on the planarized structure and having a second **opening**, and forming a second planarized structure in the second **opening**.

DETAILED DESCRIPTION - Formation of electrical metal fuse (30) involves forming a first **patterned dielectric** layer (12, 16) on a substrate and having first **opening**(s) exposing at least a portion of the substrate, forming at least a first planarized structure in the first **opening** (18), forming a second **patterned dielectric** layer on the planarized structure and having a second **opening** exposing at least a portion of the first planarized structure, and forming a second planarized structure in the second **opening**. The two planarized structures comprise the electrical metal fuse having a middle portion (34) with a thickness and a width (33, 35) between two end portions (32). The thickness and width of the middle portion is less than that of the end portions.

USE - For forming an electrical metal fuse.

ADVANTAGE - The process does not require a laser to program the fuses, requires a smaller **space** by the stacking of the end fuse portions to create thicker end fuse portions, and simply produces a more reliable fuse without additional masking. The fuse widths can be reduced due to the stacking of the end fuse portion.

DESCRIPTION OF DRAWING(S) - The figures show the process.

Dielectric layer (12, 16)

Opening (18)

Metal fuse (30)

End portions (32)

Middle portion (34)

pp; 9 DwgNo 3, 4/12

Title Terms: ELECTRIC; METAL; FUSE; PRODUCE; COMPRISE; FORMING; FIRST; PATTERN; DIELECTRIC; LAYER; SUBSTRATE; FIRST; PLANE; STRUCTURE; SECOND; PATTERN; DIELECTRIC; LAYER; SECOND; PLANE; STRUCTURE

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11/3,AB,DE/3

DIALOG(R)File 350:**Derwent WPIX**

WPI Acc No: 2002-572764/200261

Fabrication of wire bonds on pure copper damascene for e.g. complementary metal oxide semiconductor devices, involves forming aluminum-copper bond alloy on top of underlying copper pad metal

Patent Assignee: CHARTERED SEMICONDUCTOR MFG LTD PTE (CHAR-N)

Inventor: CHOOI S; HONG S; ZHOU M S

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6376353	**B1**	**20020423**	**US 2000609167**	**A**	**20000703**	**200261**	**B**

Abstract (Basic):

NOVELTY - Wire bonds are fabricated on pure copper damascene by forming aluminum-copper bond alloy on top of underlying copper pad metal.

DETAILED DESCRIPTION - Fabrication of wire bonds involves:

(1) depositing a passivating layer over a first level of conducting wiring (4) defined and over a substrate (1) wafer or module;

(2) depositing two insulating layers forming intermetal

dielectric (IMD) layers, **patterning** and etching the intermetal dielectric layers (14, 16) and passivating layer to form a **dual damascene** trench (20)/**via** (19) **opening** exposing regions of the conducting wiring;

(3) depositing and patterning a cap layer over the second IMD layer;

(4) depositing a first blanket conductive metal barrier layer or first barrier layer over the patterned cap layer and into the trench/**via openings** and over the exposed regions of the conducting wiring;

(5) depositing a blanket copper layer over the first barrier layer and filling the trench/**via opening;**

(6) polishing back by chemical mechanical polishing (CMP) the excess copper and first barrier layer material (13) stopping on the cap layer to form a **dual damascene** inlaid copper in trench/**via opening;**

(7) selectively wet etching the top layer of the inlaid copper to form a recessed copper and partially recessed trench/**via opening;**

(8) etching copper oxide on the top layer of the recessed copper by hydrogen ammonia or ammonia plasma gas treatment;

(9) depositing a second blanket conductive metal barrier layer or second barrier layer (33) over the recessed copper and patterned cap layer;

(10) depositing a blanket layer of aluminum-copper alloy (26, 34) over the second barrier layer and filling partially recessed trench/**via opening;**

(11) annealing thermally with forming gas the alloy; and

(12) polishing back by CMP the alloy and second barrier layer material stopping on the cap layer (17, 27) to form a region of inlaid alloy.

USE - For fabricating wire bonds on pure copper damascene used for metal oxide field effect transistor and complementary metal oxide semiconductor devices and for both memory and logic device applications.

ADVANTAGE - The invention improves wire bond adhesion to the bond pad and prevents peeling during wire bond adhesion tests. It has very low failure rates and shows a high reliability, as tested by gold wire bond pull tests. It is free from stress-attack, corrosion, peeling, interface failure and adhesion failures. The top aluminum-copper bond layer can be soldered without the need for further passivation.

DESCRIPTION OF DRAWING(S) - The figures show cross-sectional views of the invention.

Substrate (1)
Wiring (4)
First barrier layer material (13)
Intermetal dielectric layers (14, 16)
Cap layer (17, 27)
Via (19)
trench (20)
Aluminum-copper alloy (26, 34)
Second barrier layer (33)
pp; 18 DwgNo 3d, 4d/5

Title Terms: FABRICATE; WIRE; BOND; PURE; COPPER; COMPLEMENTARY; METAL; OXIDE; SEMICONDUCTOR; DEVICE; FORMING; ALUMINIUM; COPPER; BOND; ALLOY; TOP; UNDERLYING; COPPER; PAD; METAL

+=+

11/3,AB,DE/4
DIALOG(R)File 350:**Derwent WPIX**

014572174
WPI Acc No: 2002-392878/200242
Reduction of etching of seed layer by plating solution, comprises diminishing etching power of plating solution prior to exposing seed layer to plating solution and initiating plating current
Patent Assignee: ANDRICACOS P C (ANDR-I); HORKANS W J (HORK-I); KWIETNIAK K T (KWIE-I); LOCKE P S (LOCK-I); UZOH C E (UZOH-I)
Inventor: ANDRICACOS P C; HORKANS W J; KWIETNIAK K T; LOCKE P S; UZOH C E

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020027082	**A1**	**20020307**	**US 99387856**	**A**	**19990901**	**200242**	**B**
			US 2001983235	**A**	**20011023**		

Abstract (Basic):

NOVELTY - Reduction of etching of a seed layer by a plating solution, comprises diminishing an etching power of the plating solution prior to exposing the seed layer to the plating solution and initiating a plating current.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(A) a method of electroplating **interconnecting** structures on a semiconductor wafer comprising depositing a layer of dielectric material on a surface of a semiconductor wafer comprising integrated circuits; **patterning** the layer of **dielectric** material exposing a portion of the semiconductor wafer, the patterning matching a desired pattern of **interconnect** structures to be deposited on the semiconductor wafer; depositing a layer of a barrier material over the **patterned** layer of **dielectric** material; depositing an electrically conducting seed layer on the layer of barrier material; introducing the wafer into a plating solution; diminishing an etching power of the plating solution; initiating a plating current to electrodeposit at least one metal over the entire surface of the seed layer; and removing an overburden of electroplating metal and the seed layer and barrier layer lying on top of the layer of dielectric material;

(B) a deaerated plating solution comprising at least one metal to be plated on a seed layer; at least one acid; and a level of dissolved oxygen less than 10 to the power -7 to 5 x 10 to the power -6 moles/liter; and

(C) a plating tool comprising a plating cell (2); a plating solution reservoir (1); supply line (3) for feeding plating solution from the plating solution reservoir to the plating cell; return line (4) for feeding plating solution from the plating cell to the plating solution reservoir; and an inert gas supply for introducing inert gas into the plating solution.

USE - The method is used for reducing etching of a seed layer by a plating solution. It is favorable for use in electroplating of copper in back end of line (BEOL) structures, and may be used in any metal plating operation. It is particularly useful for use in applications where copper **interconnections** are to be deposited by electroplating on a seed layer on a semiconductor wafer including integrated circuits.

ADVANTAGE - The method improves the reliability of electrical

contact to a seed layer for plating and protecting the electrical contact to the seed layer. It can minimize chemical attack on seed layers, particularly in metal lines and trenches that can occur in the plating bath before the current is engaged. It prevents dissolution of conducting seed layer that can occur in the vicinity of the electrical contacts to a semiconductor wafer surface. It permits use of very thin seed layers in the damascene fabrication techniques for on-chip **interconnections** using electroplated copper. It protects very thin current-carrying layers from attack by the plating solution in the period before the plating current is applied.

DESCRIPTION OF DRAWING(S) - The figure represents a schematic drawing illustrating a plating system including elements for eliminating dissolved oxygen from a plating bath.

Reservoir (1)
Plating cell (2)
Supply line (3)
Return line (4)
pp; 8 DwgNo 2/2

Title Terms: REDUCE; ETCH; SEED; LAYER; PLATE; SOLUTION; COMPRISE; DIMINISH ; ETCH; POWER; PLATE; SOLUTION; PRIOR; EXPOSE; SEED; LAYER; PLATE; SOLUTION; INITIATE; PLATE; CURRENT

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11/3,AB,DE/5
DIALOG(R)File 350:**Derwent WPIX**

WPI Acc No: 2002-289562/200233
Method of forming conductive lines of semiconductor device
Patent Assignee: HYNIX SEMICONDUCTOR INC (HYNI-N)
Inventor: KIM J H

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2001061124	**A**	20010707	KR 9963610	A	19991228	200233	B

Priority Applications (No Type Date): KR 9963610 A 19991228

Abstract (Basic):

NOVELTY - A conductive line forming method for semiconductor device is provided to enhance the features and reliability of a semiconductor device by forming a conductive lines using a **dual damascene** technique for avoiding dishing or erosion.

DETAILED DESCRIPTION - A semiconductor substrate(21) is provided with an **oxide film** line/**space pattern**. A tungsten film(23) is formed on the whole surface of the semiconductor substrate(21) to fill between the line/**space** pattern. The tungsten film(23) is flattened through Chemical Mechanical Polishing (CMP) using slurry. The slurry has a ratio to deionized water of 100 to 500 : 1, or to a hydrogen peroxide of 50 to 100 : 1, and pH of 2 to 4. KOH or NH4OH is added to the slurry to prevent agglomeration of polishing particles.

pp; 1 DwgNo 1/10

Title Terms: METHOD; FORMING; CONDUCTING; LINE; SEMICONDUCTOR; DEVICE

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11/3,AB,DE/7
DIALOG(R)File 350:**Derwent WPIX**

WPI Acc No: 2001-540102/200160

Method for manufacturing **dual damascene** structure comprises forming trench, forming cavity under trench, forming **opening** under cavity, forming metal layer on second dielectric and filling trench, cavity and **opening**

Patent Assignee: UNITED MICROELECTRONICS CORP (UNMI-N)

Inventor: LAI Y

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
TW 429572	**A**	20010411	TW 99113863	A	19990813	200160	**B**

Abstract (Basic):

NOVELTY - Method for manufacturing **dual damascene** structure comprises: forming trench through second dielectric and mask to expose first **dielectric**; forming **patterned** photoresist on second **dielectric**; etching to form a cavity under trench in the first dielectric; etching first dielectric to form an **opening** under cavity; forming metal layer on second dielectric; and filling trench, cavity and **opening**.

DETAILED DESCRIPTION - Method for manufacturing **dual damascene** structure comprises:

(a) sequentially forming a first dielectric, a mask and a second dielectric on substrate;

(b) removing part of the second dielectric and part of the mask until surface of the first dielectric is exposed to form a trench;

(c) forming a patterned photoresist layer on the second dielectric;

(d) conducting isotropic etching to form a cavity under the trench in the first dielectric in which the width of the cavity is smaller than the width of the trench;

(e) conducting anisotropic etching to etch the first dielectric to form an **opening** under the cavity; and

(f) after removing the photoresist, forming a metal layer on the second dielectric and filling up the trench, the cavity and the **opening**.

USE - None given.

ADVANTAGE - Generation of voids is decreased in order to increase the reliability of the **dual damascene** structure.

DwgNo 0/1

Title Terms: METHOD; MANUFACTURE; DUAL; STRUCTURE; COMPRISE; FORMING; TRENCH; FORMING; CAVITY; TRENCH; FORMING; **OPEN**; CAVITY; FORMING; METAL; LAYER; SECOND; DIELECTRIC; FILL; TRENCH; CAVITY; **OPEN**

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11/3,AB,DE/8

DIALOG(R)File 350:**Derwent WPIX**

WPI Acc No: 2001-535007/200159

Fabrication of **dual damascene** structures useful in, e.g., integrated circuit microelectronic fabrications, involves employing spin-on polymer etch stop layer

Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)

Inventor: JANG S

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6265319	**B1**	**20010724**	**US 99387440**	**A**	**19990901**	**200159**	**B**

Abstract (Basic):

NOVELTY - A **dual damascene** structure is fabricated by

employing spin-on polymer etch stop layer.
DETAILED DESCRIPTION - Formation of a **dual damascene** structure comprises (a) forming a first dielectric layer (14') over a substrate (10) having contact regions (12a-c); (b) forming an intermediate carbon-containing low dielectric constant dielectric layer (16'), upon the first dielectric layer; (c) forming a second dielectric layer (18'), upon the intermediate dielectric layer; (d) forming a first patterned photoresist etching mask layer which defined contact **via** holes, over the second dielectric layer; (e) etching through the first patterned photoresist mask layer employing a first anisotropic reactive etch process, and transferring the pattern into and through the second dielectric layer, intermediate dielectric constant dielectric layer, and first dielectric layer; (f) stripping the first patterned photoresist etch mask layer; (g) forming a second patterned photoresist etch mask layer defining a trench pattern, over the substrate; (h) etching through the second patterned photoresist etch mask layer employing a second anisotropic reactive etch process, and transferring the trench **pattern** into the second **dielectric** layer, using the intermediate dielectric layer as an etch stop layer, thus forming an etched contact **via** hole and trench pattern; and (i) striping the second patterned photoresist etch mask layer.
USE - For forming **dual damascene** structures, i.e., metal **interconnection** layers useful in microelectronic fabrications, such as, integrated circuit microelectronic fabrications, charge coupled device microelectronic fabrications, light emitting diode microelectronic fabrications, and flat panel display microelectronic fabrications (claimed).
ADVANTAGE - The invention provides a **dual damascene** stacked conductor **interconnection** layer with reduced inter-level capacitance and lowered electrical resistance.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional schematic view of the **dual damascene** structure.
Substrate (10)
Contact regions (12a-c)
First dielectric layer (14')
Intermediate dielectric layer (16')
Second dielectric layer (18')
Conductor material (28)
Dual damascene interconnection layer (29)
pp; 13 DwgNo 4/12
Title Terms: FABRICATE; DUAL; STRUCTURE; USEFUL; INTEGRATE; CIRCUIT; MICROELECTRONIC; FABRICATE; EMPLOY; SPIN; POLYMER; ETCH; STOP; LAYER

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11/3,AB,DE/9
DIALOG(R)File 350:**Derwent WPIX**

WPI Acc No: 2001-334459/200135
Dual-damascene process involves forming first **dielectric** layer, stop layer **pattern** and second **dielectric** layer on wafer, etching these layers to form **via**, forming conductor on wafer and chemical mechanical polishing to form conductive wires
Patent Assignee: IND TECHNOLOGY RES INST (INTE-N)

Inventor: TSUEI B

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
TW 417248	**A**	20010101	TW 99120383	A	19991118	200135	B

Abstract (Basic):

NOVELTY - **Dual-damascene** process comprises: forming a first dielectric layer; forming a stop layer **pattern**; forming a second **dielectric** layer on first dielectric layer; etching second **dielectric** layer, stop layer **pattern** and first **dielectric** layer to form a first **via**; etching second dielectric layer and forming a conductor on wafer; and performing chemical mechanical polishing to form conductive wires.

DETAILED DESCRIPTION - **Dual-damascene** process comprises:

(a) forming a first dielectric layer on the insulation layer and the lower conductive pattern of a wafer;

(b) forming an etching stop layer and removing most of the etching stop layer, thereby forming a stop layer pattern, which is placed just above the lower conductive **pattern** with the first **dielectric** layer arranged in between;

(c) forming a second dielectric layer on the first dielectric layer to cover the stop layer pattern, in which the etched stop layer has a dielectric constant larger than those of the first and second dielectric layers;

(d) etching the second dielectric layer, the stop layer **pattern** and the first **dielectric** layer to form a first **via** for exposing a part of the lower conductive pattern;

(e) etching the second dielectric layer and forming a conductive substance on the whole wafer, so as to form conductor on the part of the wafer that is not covered by the second **dielectric** **pattern**; and

(f) performing a chemical mechanical polishing process to form conductive wires, so that only a part of the lower portion of the conductive layer has etching stop layer.

USE - None given.

ADVANTAGE - The capacitance effect caused by etching stop layer is decreased.

DwgNo 0/1

Title Terms: DUAL; PROCESS; FORMING; FIRST; DIELECTRIC; LAYER; STOP; LAYER; PATTERN; SECOND; DIELECTRIC; LAYER; WAFER; ETCH; LAYER; FORM; FORMING; CONDUCTOR; WAFER; CHEMICAL; MECHANICAL; POLISH; FORM; CONDUCTING; WIRE

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11/3,AB,DE/10

DIALOG(R)File 350:**Derwent WPIX**

WPI Acc No: 2001-315694/200133

Deposition of copper seed layer involves providing dielectric layer overlying semiconductor substrate, **patterning dielectric** layer, depositing barrier and copper seed layers, and performing electroless plating

Patent Assignee: CHARTERED SEMICONDUCTOR MFG LTD PTE (CHAR-N)

Inventor: GUPTA S; KEUNG P H K; RAMASAMY C; SHENG Z M; HO P K K; ZHOU M S

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6225221	**B1**	**20010501**	**US 2000501966**	**A**	**20000210**	**200133**	**B**
SG 93880	A1	20030121	SG 20004601	A	20000817	200319	

Abstract (Basic):
NOVELTY - A copper seed layer is deposited by providing dielectric layer overlying a semiconductor substrate; **patterning** the **dielectric** layer to form trenches; depositing barrier layer overlying the dielectric layer; depositing a copper seed layer overlying the barrier layer; and performing electroless plating using copper seed layer to complete the integrated circuit (IC) device.

DETAILED DESCRIPTION - Deposition of a copper (Cu) seed layer (38) comprises:

(i) providing a dielectric layer (30) overlying a semiconductor substrate (28);

(ii) **patterning** the **dielectric** layer to form trenches for planned **dual damascene interconnects**;

(iii) depositing a barrier layer (34) overlying the dielectric layer;

(iv) depositing a Cu seed layer overlying the barrier layer by the reaction of copper (II) fluoride gas with the barrier layer; and

(v) performing electroless plating using Cu seed layer to complete the IC device.

USE - For depositing a Cu seed layer for electroless Cu plating in the fabrication of **dual damascene interconnects** for the manufacture of IC devices.

ADVANTAGE - The method deposits a Cu seed layer more conformally than physical vapor deposition. It does not require expensive precursors, it is faster and cleaner than electroless plating, and does not require induction layers to plate. The seed layer can be kept very thin while still covering the steps.

DESCRIPTION OF DRAWING(S) - The figure schematically illustrates a cross-section of IC device.

Semiconductor substrate (28)
Dielectric layer (30)
Barrier layer (34)
Cu seed layer (38)
pp; 8 DwgNo 3/5

Title Terms: DEPOSIT; COPPER; SEED; LAYER; DIELECTRIC; LAYER; OVERLIE; SEMICONDUCTOR; SUBSTRATE; PATTERN; DIELECTRIC; LAYER; DEPOSIT; BARRIER; COPPER; SEED; LAYER; PERFORMANCE; ELECTROLESS; PLATE

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11/3,AB,DE/11
DIALOG(R)File 350:**Derwent WPIX**

WPI Acc No: 2001-257003/200126
Dual damascene copper **interconnect** formed by depositing copper on barrier layer formed over metal layer with **via pattern** formed in **dielectric** using SiN as etch stop
Patent Assignee: TAIWAN SEMICONDUCTOR CO (TASE-N)
Inventor: LIU C

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6211085	**B1**	**20010403**	**US 99252491**	**A**	**19990218**	**200126**	**B**

Abstract (Basic):
NOVELTY - **Dual damascene** copper **interconnect** is formed by depositing dielectric and then a SiN layer by PE-CVD. A **via** pattern is formed by etching through the second dielectric layer and a conducting line pattern is formed using SiN as etch stop.

Metal layer (80), barrier (90) and copper seed barrier are deposited. Copper (94) is deposited by electroplating and then planarized. Thickness of second dielectric layer is greater than first.

USE - Formation of **interconnect** of semiconductor device.

ADVANTAGE - The method does not involve CVD of tungsten at the contact level and does not require CMP.

DESCRIPTION OF DRAWING(S) - The figure shows three process steps.

Metal (80)
Barrier (90)
Copper (94)
pp; 8 DwgNo 4,5,6/6

Title Terms: DUAL; COPPER; **INTERCONNECT**; FORMING; DEPOSIT; COPPER; BARRIER; LAYER; FORMING; METAL; LAYER; PATTERN; FORMING; DIELECTRIC; ETCH ; STOP

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11/3,AB,DE/12
DIALOG(R)File 350:**Derwent WPIX**

WPI Acc No: 2001-256681/200126 Related WPI Acc No: 1999-468454
Formation of contact level **dual damascene** on silicon substrate uses titanium aluminum nitride barrier layer, and aluminum wetting layer between the barrier layer and copper layer
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: MCTEER A

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6204179	**B1**	**20010320**	**US 9838221**	**A**	**19980311**	**200126**	**B**
				Cont of patent US 5939788			

Abstract (Basic):

NOVELTY - A contact level **dual damascene** is formed on a silicon substrate (10) by providing two insulating layers (7, 9) on the substrate with an **opening**, depositing a refractory metal layer on inside surfaces of the **opening**, depositing a barrier layer (4) on the metal layer, depositing a wetting layer on the barrier layer, and depositing a copper layer (3) on the wetting layer to fill the **opening**.

USE - For forming a contact level **dual damascene** on a silicon substrate useful in very large-scale integrated circuit.

ADVANTAGE - The invention provides a barrier layer that is stable to high temperatures required to reflow copper after physical vapor deposition, and an aluminum wetting layer that effectively lowers the temperature at which the copper reflows and allows the use of typical barrier layers.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of a contact level **dual damascene**.

Copper layer (3)
Barrier layer (4)
Copper aluminum alloy (6)
Insulating layers (7, 9)
Silicon substrate (10)
Refractory metal silicide (11)
Refractory metal layer (13)
pp; 23 DwgNo 6/16

Title Terms: FORMATION; CONTACT; LEVEL; DUAL; SILICON; SUBSTRATE; TITANIUM; NITRIDE; BARRIER; LAYER; WET; LAYER; BARRIER; LAYER; COPPER; LAYER

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11/3,AB,DE/13
DIALOG(R)File 350:**Derwent WPIX**

WPI Acc No: 2001-181864/200118
Creation of a copper **dual damascene** structure comprises forming copper seed layer inside **opening** and over intermetal dielectric, filling **opening** with spin-on material, and removing seed layer over dielectric
Patent Assignee: CHARTERED SEMICONDUCTOR MFG PTE LTD (CHAR-N); CHARTERED SEMICONDUCTOR MFG LTD PTE (CHAR-N); CHARTERED SEMICONDUCTOR MFG LTD
Inventor: GUPTA S; KWOK KEUNG HO P; SHENG ZHOU M; HO P K K; ZHOU M S

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6184138	**B1**	**20010206**	**US 99390782**	**A**	**19990907**	**200118**	**B**

Abstract (Basic):

NOVELTY - Creation of a copper **dual damascene** structure comprises forming a copper seed layer inside **dual damascene** **opening** and over surface of inter-metal dielectric (IMD), filling **opening** with spin-on material, removing the seed layer above the IMD, removing the spin-on material, and electrolessly depositing copper layer over the **opening**.

DETAILED DESCRIPTION - Creation of a copper **dual** **damascene** structure on the surface of a semiconductor substrate comprises forming an **opening** for a **dual damascene** structure on the surface of the substrate in a layer of inter-metal dielectric (IMD) (16) over which a cap layer (18) has been deposited. The surface of the substrate contains metal contact points. A diffusion barrier layer (20) is deposited inside the **opening** and over the surface of the surrounding area. A copper seed layer (26) is deposited over the diffusion barrier layer. A spin-on layer is deposited over the copper seed layer. The spin-on material is removed from above the **opening** and from above the surface of the surrounding area. The spin-on material is left in place inside the **opening** of the **dual damascene** structure. The copper seed layer and barrier layer are each removed from above the surface of the surrounding area. The spin-on material is removed from the **opening** of the **dual damascene** structure. A layer of copper is selectively electroless deposited over the **dual damascene opening** . The excess copper is removed from above the **dual** **damascene opening** by a touch-up chemical-mechanical polishing (CMP). An oxidation/diffusion protection layer (30) is deposited over the surface of the **dual damascene** structure and its surrounding area.

USE - For creating a copper **dual damascene** structure on the surface of a semiconductor substrate.

ADVANTAGE - The method reduces surface dishing and erosion in the copper surface of a **dual damascene** structure and improves global planarity and uniformity of the copper surfaces of **dual** **damascene** structures.

DESCRIPTION OF DRAWING(S) - The drawings show cross-sections of a copper **dual damascene** structure, at different process stages.

IMD layer (16)

cap layer (18)
barrier layer (20)
copper seed layer (26)
oxidation/diffusion protection layer (30)
pp; 9 DwgNo 5,6,7/7

Title Terms: CREATION; COPPER; DUAL; STRUCTURE; COMPRISE; FORMING; COPPER; SEED; LAYER; **OPEN**; DIELECTRIC; FILL; **OPEN**; SPIN; MATERIAL; REMOVE; SEED; LAYER; DIELECTRIC

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11/3,AB,DE/14
DIALOG(R)File 350:**Derwent WPIX**

WPI Acc No: 2001-137245/200114 Related WPI Acc No: 1999-619684
Formation of **dual damascene** pattern used in integrated chip manufacture involves providing substrate having composite insulation layer, patterning a photoresist layer using phase-shift mask, and depositing metal into the trench and the hole
Patent Assignee: IND TECHNOLOGY RES INST (INTE-N)
Inventor: DAI C

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6180512	**B1**	**20010130**	**US 97949353**	**A**	**19971014**	**200114**	**B**
			US 99359903	**A**	**19990726**		

Abstract (Basic):

NOVELTY - A **dual damascene** pattern is formed by providing a substrate with deposited composite insulation layer; patterning the photoresist layer using a phase-shifting mask; forming a patterned photoresist layer; performing wet development; transferring the hole pattern and the line **pattern** into the **dielectric** layer; removing the photoresist layer; and depositing metal into trench and hole.

DETAILED DESCRIPTION - Formation of a **dual damascene** pattern employing single photoresist layer comprises: providing a substrate (150) with deposited composite insulation layer comprising two dielectric layers (160, 180); forming a photoresist layer on the composite layer; patterning the photoresist layer by exposing it using a phase-shifting mask comprising hole and line patterns and followed by baking; performing a wet development to form a patterned photoresist layer; etching the second layer of the dielectric using the photoresist layer as mask thus transferring the hole **pattern** into the intermediate **dielectric** layer (170); etching photoresist to extend downward; etching the composite insulation layer thus transferring the line **pattern** into the second **dielectric** layer to form a line trench, and transferring the hole pattern in to the first dielectric layer to form a hole; removing the photoresist layer; and depositing metal (200, 210) into the trench and the hole to form a **dual damascene** structure.

USE - The method is used for forming **dual damascene** patterns or for the fabrication of metal lines and **vias** in a semiconductor substrate. The method is used for formation of ultra large scale (ULSI) integrated chips.

ADVANTAGE - The method is simple and improves the alignment of wiring layer to the underlying **interconnect** hole pattern. It reduces overlay tolerances and process bias thus increases the packing density of ultra large scaled integrated chips.

DESCRIPTION OF DRAWING(S) - The figure is a partial cross-sectional view of a semiconductor substrate with metal deposited in the trench and in the hole.

Substrate (150)

Dielectric layers (160, 170, 180)

Metal (200, 210)

pp; 12 DwgNo 4h/4

Title Terms: FORMATION; DUAL; PATTERN; INTEGRATE; CHIP; MANUFACTURE; SUBSTRATE; COMPOSITE; INSULATE; LAYER; PATTERN; PHOTORESIST; LAYER; PHASE ; SHIFT; MASK; DEPOSIT; METAL; TRENCH; HOLE

+=+

11/3,AB,DE/15

DIALOG(R)File 350:**Derwent WPIX**

WPI Acc No: 2000-678770/200066

Related WPI Acc No: 2001-266387; 2001-397185; 2003-635865

Seed layers for semiconductor **interconnects** for thin head films or micromachined Microelectromechanical Systems devices

Patent Assignee: COHEN U (COHE-I)

Inventor: COHEN U

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6136707	**A**	**20001024**	**US 99410898**	**A**	**19991002**	**200066**	**B**

Abstract (Basic):

NOVELTY - Electroplating metals or alloys for filling high aspect ratio **openings** e.g trenches and **vias,** for semiconductor metallisation **interconnects,** thin film heads,or micromachined Microelectromechanical Systems devices.

DETAILED DESCRIPTION - Production of metallic **interconnects** comprises:

(1) forming a **patterned insulating** layer on a substrate, the **patterned insulating** layer including at least one **opening** with a surrounding field;

(2) depositing a barrier layer over the field and inside surfaces of the **opening**(s);

(3) depositing a first seed layer over the barrier layer using first deposition technique;

(4) depositing a second seed layer over the first using second deposition technique;

(5) electroplating a metallic layer over the scond seed layer, comprising copper, silver, or alloy containing one of these metals.

USE - Electroplating of tenches or **vias** for semiconductor **interconnects.**

ADVANTAGE - The improved seed layers provide reliable void-free filling of small **openings** with high aspect ratios for (**Dual**) **Damascene** copper and/or silver **interconnects.**

DESCRIPTION OF DRAWING(S) - Cross-sectional view of structure.

barrier layer (18)

wafer surface (10)

patterned insulation layer (12)

opening (16)

conformal seed layer (20)

non-conformal seed layer (22)

interconnect (24)

pp; 9 DwgNo 2/4

Title Terms: SEED; LAYER; SEMICONDUCTOR; **INTERCONNECT**; THIN; HEAD; FILM; SYSTEM; DEVICE

+=+

11/3,AB,DE/16

DIALOG(R)File 350:**Derwent WPIX**

WPI Acc No: 2000-586367/200055

Formation of damascene structures used in ultra large scale integrated circuit chips involves forming a seed layer **via** tungsten chemical vapor deposition process

Patent Assignee: IND TECHNOLOGY RES INST (INTE-N)

Inventor: CHEN H; LOU C

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6110826	**A**	**20000829**	**US 9892816**	**A**	**19980608**	**200055**	**B**

Abstract (Basic):

NOVELTY - **Dual damascene** structure is formed by forming a seed layer in a selected portion of a structure **via** selective tungsten chemical vapor deposition.

DETAILED DESCRIPTION - Formation of a **dual damascene** structure using selective tungsten chemical vapor deposition (W CVD) comprises:

(a) forming an interlevel dielectric (ILD) layer (600) over a semiconductor substrate (100) having active and passive regions;

(b) forming an etch-stop layer (650) over the ILD layer and an intermetal dielectric (IMD) layer (700) over the etch-stop layer;

(c) forming a first photoresist layer over the IMD layer and patterning with a mask containing a line trench pattern;

(d) etching through the line trench pattern to form the line trench pattern into the IMD layer and then removing the first photoresist layer;

(e) forming a seed layer (800) over the IMD layer including the line trench (725) with sidewall (850) and flat bottom (875);

(f) removing the seed layer from the surface of the IMD layer;

(g) forming a second photoresist over the IMD layer and the line trench and patterning with a mask having a contact hole pattern;

(h) etching through the contact hole pattern to form the contact hole **pattern** into the **ILD** layer;

(i) removing the second photoresist layer and cleaning the contact hole;

(j) depositing a selective W CVD in the line trench and contact hole composite structure; and

(k) performing chemical mechanical polish to planarize and to complete the fabrication of the semiconductor substrate.

USE - For forming **dual damascene** structure useful in ultra large scale integrated circuit chips.

ADVANTAGE - Provides contact holes and **via** holes with free voids.

DESCRIPTION OF DRAWING(S) - The drawing shows a **dual damascene** structure.

semiconductor substrate (100)

ILD layer (600)

etch-stop layer (650)

IMD layer (700)

pp; 11 DwgNo 4f/4

Title Terms: FORMATION; STRUCTURE; ULTRA; SCALE; INTEGRATE; CIRCUIT; CHIP; FORMING; SEED; LAYER; TUNGSTEN; CHEMICAL; DEPOSIT; PROCESS

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11/3,AB,DE/17

DIALOG(R)File 350:**Derwent WPIX**

WPI Acc No: 2000-422094/200036

Fabrication of metal line using deposition process involves providing **insulating** layer with trenches, **patterning** a seed layer, depositing a metal, and chemical-mechanical polishing

Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)

Inventor: JANG S

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6071814	**A**	**20000606**	**US 98161566**	**A**	**19980928**	**200036**	**B**

Abstract (Basic):

NOVELTY - Metal line is fabricated by providing an insulating layer with trenches defined by sidewalls and a bottom, patterning a seed layer to form a seed layer lip, depositing metal, and chemical-mechanical polishing the metal and seed layer lip.

DETAILED DESCRIPTION - A metal line (50) is fabricated by:

providing an insulating layer (20) having trenches (24) arranged in a pattern where each trenches is defined by sidewalls and a bottom; forming a seed layer (30B) over the insulating layer, sidewalls, and the bottom of each trench;

patterning a top seed layer portion by removing portions of the seed layer to form seed layer lips (30C) adjacent a trench seed layer portion so that the remaining seed layer electrically connects the trench seed layers in the trenches;

depositing a metal on the top seed layer, the seed layer lips, and the trench seed layer portion filling the trenches; and

chemical-mechanically polishing the metal and the seed layer lips to remove excess metal and the seed layer lips and forming a metal line pattern filling the trenches.

The seed layer comprises trench seed layer portion covering the sidewalls and bottoms of the trenches. The top seed layer portion covers the insulating layer top surfaces.

USE - For fabricating a metal line using deposition process.

ADVANTAGE - The invention is faster and easier because the field areas are not covered with metal. The remaining metal on the insulating layer can be polished off faster and eliminates dishing.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of forming and patterning a seed layer.

Insulating layer (20)
Trench (24)
Seed layer (30B)
Seed layer lips (30C)
Metal line (50)
pp; 8 DwgNo 4/6

Title Terms: FABRICATE; METAL; LINE; DEPOSIT; PROCESS; INSULATE; LAYER; TRENCH; PATTERN; SEED; LAYER; DEPOSIT; METAL; CHEMICAL; MECHANICAL; POLISH

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11/3,AB,DE/18

DIALOG(R)File 350:**Derwent WPIX**

012901130
WPI Acc No: 2000-072966/200006
Forming an **interconnect** structure for an integrated circuit device
Patent Assignee: CONEXANT SYSTEMS INC (CONE-N); NEWPORT FAB LLC (NEWP-N)
Inventor: BRONGO M R; ZHAO B

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9963591	A1	19991209	WO 99US11410	A	19990526	200006	B
EP 1080495	A1	20010307	EP 99924469	A	19990526	200114	
US 6627539	**B1**	**20030930**	**US 9887116**	**P**	**19980529**	**200367**	
			US 98149910	**A**	**19980909**		

Abstract (Basic):

NOVELTY - An **interconnect** structure for an integrated circuit device is formed using two low-k dielectric layers with no chemical-mechanical polishing.

DETAILED DESCRIPTION - The method comprises: forming a planar layer of conductor and gap-fill dielectric; adding layers of, in sequence, first low-k dielectric, first cap dielectric, second low-k dielectric and second cap **dielectric; patterning** the layers into **vias** and in the first low-k dielectric layer and trenches in the second low-k dielectric layer, the first cap dielectric layer acting as an etch buffer; adding a conformal metal layer which contacts the conductor; and removing excess metal to form a planar surface.

USE - Forming an **interconnect** structure for an integrated circuit device.

ADVANTAGE - A **dual damascene** process is provided which is simple and low cost and which avoids chemical-mechanical polishing and reduces parasitic capacitance and coupling.

pp; 26 DwgNo 0/3

Title Terms: FORMING; **INTERCONNECT**; STRUCTURE; INTEGRATE; CIRCUIT; DEVICE

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11/3,AB,DE/19
DIALOG(R)File 350:**Derwent WPIX**

013539090
WPI Acc No: 2001-023296/200103 Related WPI Acc No: 2002-266554
Dual damascene process involves depositing second silicon nitride layer on exposed wiring layer, depositing barrier layer on **via** hole and trench, and over-filling the **via** hole and the trench with copper
Patent Assignee: IND TECHNOLOGY INST RES (INTE-N)
Inventor: LIN K

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6140220	**A**	**20001031**	**US 99349843**	**A**	**19990708**	**200103**	**B**

Abstract (Basic):

NOVELTY - A **dual damascene** process comprises depositing a second silicon nitride layer on an exposed wiring layer. A barrier layer is deposited covering the interior surfaces of a **via** hole and a trench. The **via** hole and the trench are over-filled with copper. The copper layer is planarized in which the trench is just filled with copper and the third silicon oxide layer is exposed.

DETAILED DESCRIPTION - A **dual damascene** process

comprises providing a partially completed integrated circuit covered by a first silicon oxide layer (11) in which a first damascene wiring layer (12) is embedded in its upper surface. A first silicon nitride layer (13) is deposited on the upper layer of the wiring, and a second silicon oxide layer (21) on the first silicon nitride layer. The second silicon **oxide layer** is **patterned** and etched to form a **via** hole (61) that extends through the first silicon nitride layer, exposing the first layer of damascene wiring. A conformal layer of second silicon nitride is deposited on the exposed wiring layer, forming a coating on all interior surfaces of the **via** hole and on the second silicon oxide layer. The coated **via** hole is over-filled with silicon oxide which forms a third silicon layer on the second silicon nitride layer. The third silicon **oxide layer** is **patterned** and etched with an etchant that attacks both silicon oxide and silicon nitride with an etching ratio of 6:1 to 15:1, oxide:nitride. A trench in the third silicon oxide layer is formed, which fully overlaps the **via** hole extending through the second silicon nitride layer to the second silicon oxide layer, and exposing the first layer of damascene wiring. A barrier layer is deposited to form a coating that covers all the interior surfaces of the **via** hole and of the trench, as well as the exposed first wiring layer, and that covers the third silicon oxide layer. The **via** hole and the trench are over-filled with copper. The copper layer is planarized in which the trench is just filled with copper and the third silicon oxide layer is exposed.

USE - For forming **dual damascene** structures.

ADVANTAGE - The invention allows the use of a barrier layer that is thinner than normal so that more copper can be included in the **via** hole, resulting in an improved conductance of the **via**.

DESCRIPTION OF DRAWING(S) - The figure illustrates the formation of a **via** hole portion of a **dual damascene** structure.

first silicon oxide layer (11)
first damascene wiring layer (12)
first silicon nitride layer (13)
second silicon oxide layer (21)
via hole (61)
pp; 9 DwgNo 6/12

Title Terms: DUAL; PROCESS; DEPOSIT; SECOND; SILICON; NITRIDE; LAYER; EXPOSE; WIRE; LAYER; DEPOSIT; BARRIER; LAYER; HOLE; TRENCH; FILL; HOLE; TRENCH; COPPER

L9 ANSWER 1 OF 3 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:575481 HCAPLUS Full-text
TI Metal-to-metal **antifuse** structure and fabrication method
IN Wang, Daniel C.
PA Actel Corporation, USA

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002100907	A1	20020801	US 2000-737642	20001214 X
				US 2000-737642 A	20001214
				WO 2001-US49300W	20011213

AB A metal-to-metal **antifuse** according to the present invention is compatible with a Cu **dual damascene** process and is formed over a lower Cu metal layer planarized with the top surface of a lower insulating layer. A lower barrier layer is disposed over the lower Cu metal layer. An **antifuse** material layer is disposed over the lower barrier layer. An upper barrier layer is disposed over the **antifuse** material layer. An upper insulating layer is disposed over the upper barrier layer. An upper Cu metal layer is planarized with the top surface of the upper insulating layer and extends to make elec. contact with the upper barrier layer.
ST copper **antifuse** semiconductor integrated circuit
IT Polishing
(chemical-mech.; metal-to-metal **antifuse** in semiconductor integrated circuit device)
IT **Antifuses**
Electric contacts
Integrated circuits
Interconnections, electric
(metal-to-metal **antifuse** in semiconductor integrated circuit device)
IT 409-21-2, Silicon carbide, processes 7440-21-3, Silicon, processes 7440-50-8, Copper, processes 7631-86-9, Silica, processes 11116-16-8, Titanium nitride 12033-62-4, Tantalum nitride 12033-89-5, Silicon nitride, processes
RL: DEV (Device component use); EPR (Engineering process); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(metal-to-metal **antifuse** in semiconductor integrated circuit device)

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L9 ANSWER 2 OF 3 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:256715 HCAPLUS Full-text
TI High density metal/insulator/metal capacitor using **dual-damascene** copper **interconnect** and fabrication for integrated circuits
IN Tsau, Liming

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002038903	A1	20020404	US 2001-971254	20011003
				US 2000-237916PP	20001003 X
	WO 2002029892	A3	20030306	WO 2001-US31140	20011003

AB A method is claimed for fabricating a MIM capacitor with fewer steps using standard materials. An electronic structure having a 1st conductive layer provided by a **dual damascene** fabrication process; an etch-stop layer provided by the fabrication process, and elec. coupled with the 1st conductive layer, the etch-stop layer having a preselected dielec. constant and a predetd. geometry; and a 2nd conductive layer, elec. coupled with the etch-stop layer. The structure can be, for example, a metal-insulator-metal capacitor, an **antifuse**, and the like.

ST MIM capacitor fabrication dielec film photolithog copper **interconnect**
IT Films
(elec. conductive; high d. metal/insulator/metal capacitor using **dual-damascene** copper **interconnect** and fabrication for integrated circuits)
IT Electric conductors
(films; high d. metal/insulator/metal capacitor using **dual-damascene** copper **interconnect** and fabrication for integrated circuits)
IT **Antifuses**
Dielectric films
Integrated circuits
Interconnections, electric
Photolithography
(high d. metal/insulator/metal capacitor using **dual-damascene** copper **interconnect** and fabrication for integrated circuits)
IT Metals, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(high d. metal/insulator/metal capacitor using **dual-damascene** copper **interconnect** and fabrication for integrated circuits)
IT Capacitors
(metal/insulator/metal; high d. metal/insulator/metal capacitor using **dual-damascene** copper **interconnect** and fabrication for integrated circuits)
IT Etching
(stop-layer; high d. metal/insulator/metal capacitor using **dual -damascene** copper **interconnect** and fabrication for integrated circuits)
IT **Interconnections**, electric
(**vias**; high d. metal/insulator/metal capacitor using **dual-damascene** copper **interconnect** and fabrication for integrated circuits)
IT 12033-89-5, Silicon nitride, processes
RL: CPS (Chemical process); DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(high d. metal/insulator/metal capacitor using **dual-damascene** copper **interconnect** and fabrication for integrated circuits)
IT 7440-50-8, Copper, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(high d. metal/insulator/metal capacitor using **dual-damascene** copper **interconnect** and fabrication for integrated circuits)

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L9 ANSWER 3 OF 3 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1997:128079 HCAPLUS Full-text
TI Making a **dual damascene antifuse** structure
IN Zheng, Jiazhen; Chan, Lap
PA Chartered Semiconductor Manufacturing Pte, Ltd., Singapore
PATENT NO. KIND DATE APPLICATION NO. DATE

PI US 5602053 A 19970211 US 1996-628068 19960408
US 5705849 A 19980106 US 1996-735060 19961018

AB An improved **antifuse** design has been achieved by providing a structure including a pair of alternating layers of Si nitride and amorphous Si sandwiched between 2 **dual damascene** connectors. The structure provides the advantage, over the prior art, that all elec. active surfaces of the fuse structure are planar, so no potential failure spots resulting from surface unevenness can be formed. A process for manufacturing the fuse structure involves fewer masking steps than related structures of the prior art.

ST **dual damascene antifuse** structure prepn

IT Polishing
(chemical-mech.; in preparation of **antifuse** structures having **dual damascene** connectors)

IT **Antifuses**
(making a **dual damascene antifuse** structure)

IT **Interconnections** (electric)
(preparation of **antifuse** structures having **dual damascene** connectors)

IT 7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(amorphous; making a **dual damascene antifuse** structure containing)

IT 7429-90-5, Aluminum, processes 7440-22-4, Silver, processes 7440-33-7, Tungsten, processes 7440-50-8, Copper, processes 12033-62-4, Tantalum nitride 12033-89-5, Silicon nitride, processes 12642-02-3 25583-20-4, Titanium nitride (TiN) 37359-53-8, Tungsten nitride
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(making a **dual damascene antifuse** structure containing)

See WPIX HIT S15, #2